Low Noise-Low Power Transimpedance Amplifier Design for Electric Field Sensing

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***Abstract*— Two 3V folded-cascode operational amplifiers with low noise and low power consumption were presented. The op-amps are suitable as preamplifiers for an electric field mill sensor interface. The two op-amps differ in their input stages, with the first one having a pmos differential pair and the second one being implemented with a rail-to-rail configuration. A noise optimization was performed for the configurations and was focused on low-frequency domain applications, where flicker noise is the main source of the noise. Advanced simulations were performed and the final circuits of the op-amps were compared in a 0.18 um CMOS process commercially available by XFAB, versus their noise performance and silicon area to cost ratio.**

Keywords—rail-to-rail, noise optimization, folded-cascode op-amp, low power consumption, low input voltage noise, noise-optimized preamplifier, electric field mill

I. Introduction

Electric field mills are instruments mainly used for measuring the static electric field in the atmosphere [1-3] or the electric field under high voltage direct-current power lines [4] in some applications. Additionally, they are used for detecting thunderstorms and lightning incidents [5] and as high-voltage DC meters [6].

An electric field mill is a rotating vane-style instrument typically fabricated with a sector-shaped multibladed rotor (shutter). The rotor periodically covers and exposes the stationary electrode vanes of a segmented sensing plate (stator) to the surrounding electric field. When the vanes of the stator are exposed to the electric field, each vane is charged. Instead, when the electrically grounded rotor blades cover the vanes of the stator, the vanes are discharged [7] and a weak current signal is generated.

The amplitude of the produced current signal is proportional to the intensity of the atmospheric electric field. To measure that amplitude, a signal processing channel interfacing the electric field mill includes an I-V conversion stage, commonly consisting of a transimpedance amplifier, and further circuitry. The application of the electric field mill operates at low frequencies. The chosen preamplifier must have a minimum contribution to the overall noise at these frequencies.

In this work, two op-amp designs with different configurations of the input stage are compared, aiming to determine the most suitable for the application of the electric mill field. The two op-amps have been noise optimized by adjusting the width and length of the MOSFETs with the higher noise contribution. Low power consumption is needed since the sensor interface will be supplied by energy harvesting systems.

II. Electric Field Mill Design

A. Electric field mill sensor

Fig. 1 shows the structure of a conventional field mill sensor.

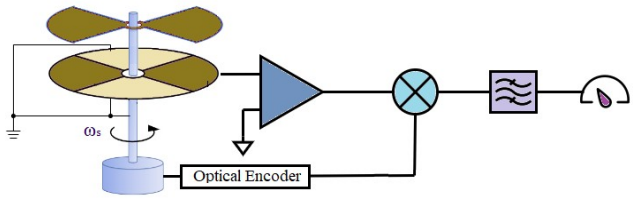

Fig. 1: Electric field mill sensor

The resulting equations for the induced charge indicate that it is proportional to the uncovered area of the vanes of the stator at each moment is provided below,

$$q(t)=\varepsilon_0 EA(t) \tag{1}$$

where ε_0 is the absolute dielectric permittivity, E is the ambient electric field intensity and $A(t)$ is the total vane area.

Knowing the equation of the induced charge, and considering a uniform field, the equation of the alternating current is given by,

$$i=\frac{dq(t)}{dt}=\varepsilon_0 E\frac{dA(t)}{dt} \tag{2}$$

The total vane area $A(t)$, changes with time according to,

$$A(t)=\begin{cases}\frac{1}{2}n\omega t\left(R^2-r^2\right), 0\le t\le\frac{T}{2}\\ \left(\frac{\pi}{2}-\frac{1}{2}n\omega t\right)\left(R^2-r^2\right), \frac{T}{2}\le t\le T\end{cases} \tag{3}$$

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where n is the number of vanes, R and r are the external and internal radius of each vane, respectively, $T=2\pi/n\omega$ and ω is the rotational speed of the motor [4, 14]. According to the above formulas, the sensing current is proportional to the vane area and the frequency of rotation.

Fig. 2 shows the electric field mill sensor interface. The resulting alternating current is passed through an I/V converter (transimpedance amplifier), which consists of the chosen preamplifier. At the output of the I/V converter, an approximately sinusoidal voltage is generated. Then, this voltage signal needs amplitude demodulation and phase discrimination of the DC electric field, so it is passed through a phase-sensitive detector. Eventually, it is filtered by a low-pass filter and ends up in an analog-to-digital converter. The obtained voltage contains information on both the intensity and the polarity of the incident electric field.

The main power consumption in electric field mill systems is due to motor operation, which typically consumes milliwatts to watts in those applications [3, 8]. In an electric field mill system, the motor and the sensor electronics would operate from a common energy source (e.g., a battery or an energy harvesting-supplied supercapacitor). Therefore the total power consumption should be kept to a minimum in to extend battery life or enable autonomous operation. A way to reduce the motor's power consumption (down to tens of milliwatts) would be using a more compact sensor design, with a smaller vane area and lower rotating frequency. But, this will lead to limited space for the sensor electronics, increased noise, and reduced sensitivity. The increase in total noise is due to the low-frequency operation of the preamplification stage, while the reduced sensitivity is due to the induced current signal's ratio to the vane area.

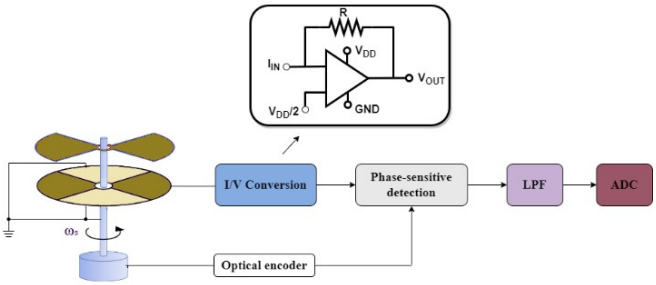


Fig. 2: Electric field mill sensor interface

B. Noise considerations

Due to the field mill application, an operational amplifier, as a preamplifier, with low input noise at voltage and current is required. Thermal and flicker noise are the primary electronic noise sources in MOSFETs for this application. Flicker noise is significantly increased at these low frequencies.

1) Thermal noise

This type of noise results from the random motion of charge carriers in an electrical conductor and shows up when there are resistive elements. Thermal noise increases with temperature, so it is proportional to absolute temperature and independent of the applied voltage or average bias current.

The thermal noise of a resistor is,

$$S=4kTR \tag{4}$$

Thermal noise is constant and independent of frequency variations, like white noise is. It drops at extremely high frequencies (terahertz), but a white spectral density is accurate for the frequency range we are interested in.

In MOSFETs, thermal noise is mainly generated by the resistance value of the channel. This noise can be modeled by a current source connected between the drain and the source, and the spectral density is,

$$\bar{I_d^2}=4kT\gamma g_m \tag{5}$$

where k is Boltzmann's constant, T is the temperature in Kelvins, γ is a coefficient and g_m is the device transconductance.

It is possible to reduce the thermal noise if we reduce the gate resistance — using fingers — when designing the layout.

2) Flicker noise

That type of noise occurs near the interface between the gate oxide and the silicon substrate due to a phenomenon by which some charge carriers get trapped and later released when they move at the interface. Thus, in the otherwise constant drain current, flicker noise is added. Flicker noise is modeled as a voltage source in series with the gate and is given by,

$$\bar{V_n^2}=\frac{K}{C_{ox}WL}\cdot\frac{1}{f} \tag{6}$$

where K is a process-dependent constant, W is the width, L is the length and C_{OX} is the gate's capacitance per unit area.

Flicker noise is inversely proportional to frequency; thus, it's also called *1/f* noise. Also, flicker noise has an inverse dependence on the width (W) and length (L) of the MOSFET. Therefore, it can be reduced by increasing the dimensions of the transistors. This results in a trade-off, as flicker noise is reduced by increasing the device area. Also, it seems that pmos transistors extract lower flicker noise than nmos.

The application of field mill operates at low frequencies, lower than 100 Hz. Thus, the flicker noise will be a lot more significant, than the thermal noise.

III. Noise Optimization

A. Operational amplifier design

To use as a preamplifier, a 3V folded cascode op-amp with a pmos differential pair is proposed. Later, it is compared with a 3V rail-to-rail folded cascode op-amp. The folded cascode op-amp is preferred, due to its high output resistance, which leads to high gain. Noise optimization for minimization of the total input noise was required.

The input differential pair consists of two matched pmos MOSFETs M0 and M1 (Fig. 3). Their sources are connected and are biased by a constant current source. The current source can be implemented by current mirrors or resistors. A higher bias current can result in a higher transconductance g_m, but then the power consumption increases. The input transistors M0 and M1 are connected to MOSFETs M6 and M7, respectively, forming M0-M6 and M1-M7 folded cascode amplifiers. These common gate transistors, M6 and M7, are biased by constant bias voltage and the resistors connected to their source terminals.

MOSFETs M16 and M17 consist of the push-pull, class AB output stage. This configuration produces a signal with low distortion when it enters the load, high efficiency, high output power, and large output swing.

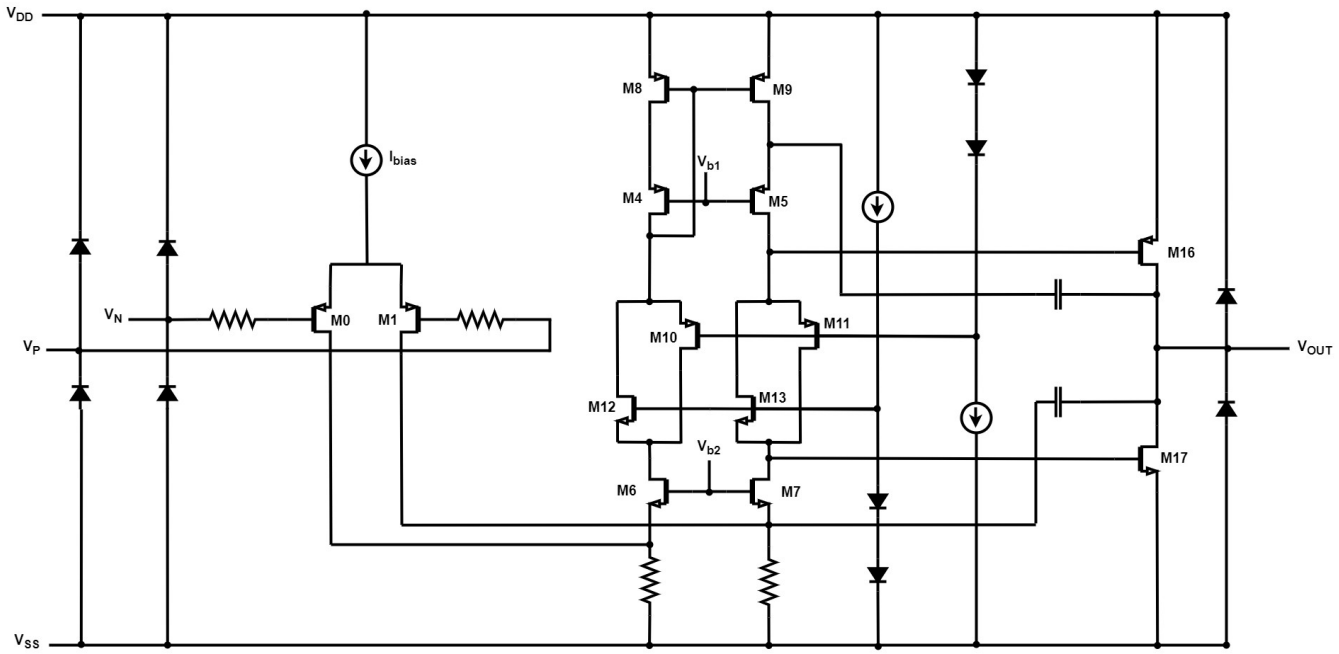


Fig. 3: Operational amplifier design

Transistors M11 and M13 form the floating class AB control and their gates are biased by the diodes D8-D9 and D6-D7 respectively. The floating class AB control biases the transistors of the push-pull (M16, M17) by keeping the voltage at their gates constant. The MOSFETs M10 and M12 have the same architecture as the floating class AB control and they are biasing the current mirror formed by M4, M5, M8, and M9, and the circuit of M6, M7, R3, and R4 that adds the signals from the input stage.

The two Miller capacitances are used for the stability of the op-amp and to determine the slew rate.

In the input stage, the diodes D0, D1, D2, and D3 and the resistors R0 and R1, along with the diodes in the output stage, D4, and D5, are used for the ESD protection of the op-amp.

After the noise optimization of this op-amp, a 3V rail-to-rail folded cascode op-amp was studied. The two circuits differ only in the input stage, where instead of a pmos differential pair, there are a pmos and a nmos differential pairs, connected in parallel. With rail-to-rail, a higher dynamic range is achieved. But with having a nmos differential pair too, the noise distortion will probably be higher.

B. *Noise optimization*

Noise optimization for the op-amp is needed due to the field mill's requirement for a low contribution to total noise. After running a noise analysis with the original dimensions of the MOSFETs, shown in Table I, the MOSFETs with the highest noise contribution were established. Noise optimization is focused on the low frequencies (< 100Hz). The noise in that frequency domain is mostly flicker noise.

A parametric analysis was held, changing the dimensions (W and L) or the number of fingers, of the said transistors and the bias current of the differential pair. After the noise optimization, other values for the bias current and the dimensions of the MOSFETs with the highest noise contribution were chosen. The new values had to be chosen carefully, trying not to increase the power consumption or the total area of the op-amp too much.

TABLE I. PMOS OP-AMP MOS DIMENSIONS PRE-OPTIMIZATION

Transistor	W/L	Transistor	W/L
M0, M1	30um/2um	M11	24um/1um
M4, M5	90um/2um	M12	13um/1um
M6, M7	30um/2um	M13	5,2um/1um
M8, M9	90um/2um	M16	120um/1um
M10	60um/1um	M17	26um/1um

1) *Transistor scaling*

The analysis prior to noise optimization shows that the MOSFETs with the highest noise contribution are M6 and M7 (at 30Hz). The differential pair M0, M1, and the transistors M8, and M9 also contribute less noise.

Using a parameter α, which varies from 1 to 6, and it's multiplied by the width and length of M6 and M7, the variations of the noise contribution of the MOSFETs, and of the total input noise are explored.

As shown in Fig. 4, when α=1, 90% of total input noise is caused by the transistors M6 and M7. As the dimensions of these transistors increase, their noise contribution decreases, while the noise contribution of the other transistors increases. Eventually, for α=6 the MOSFETs M6 and M7 contribute by 12%. As shown in Fig. 5, the total input noise is reduced too.

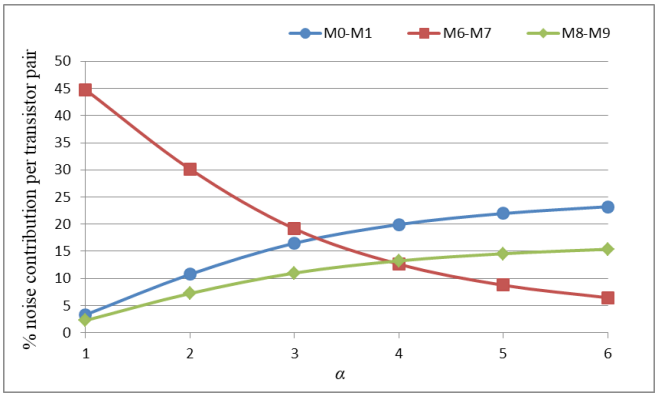


Fig. 4: % noise contribution per transistor pair VS α parameter

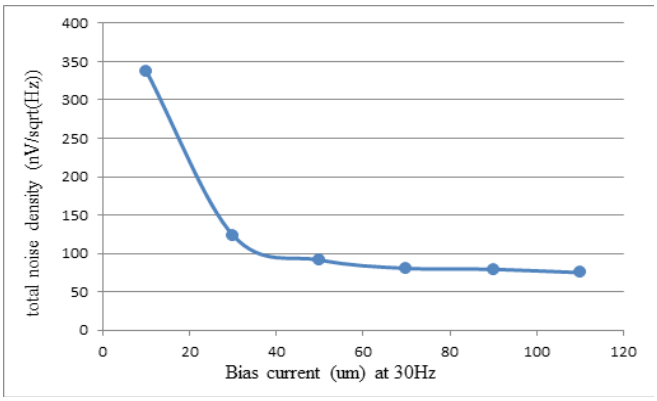


Fig. 5: total input noise density (nV/sqrt(Hz) VS α parameter at 30Hz

After the increase in the *WL* of M6-M7, the differential pair M0-M1 contributes to the total input noise the most, by 50%. So, following the same logic as before and using a parameter β, the *W* and *L* of the differential pair are altered. Fig. 6 shows the results.

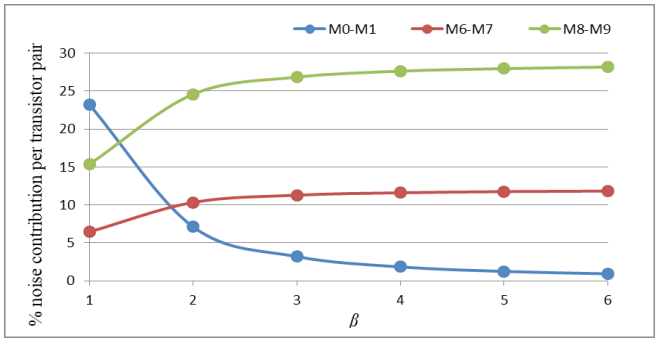


Fig. 6: % noise contribution per transistor pair VS parameter β (α=6)

2) *Number of fingers*

Another factor that affects the noise contribution is the number of fingers. The number of fingers of the differential pair M0 and M1 was increased and their noise contribution was decreased as shown in Fig. 7. As a result, the noise contribution of M8 and M9 has been increased, with these transistors being the main source of the noise.

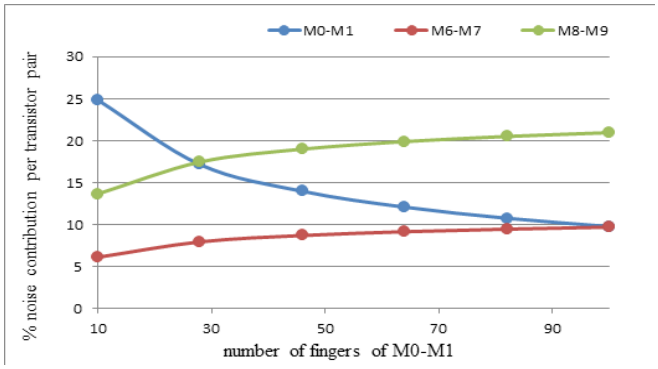


Fig. 7: % noise contribution per transistor pair VS number of fingers of M0-M1 (α=6, β=1)

Following the same logic, the values of width, length and number of fingers, of other MOSFETs with significant noise contribution can be altered.

3) *Bias current*

Another way to decrease the total input noise of the op-amp is by increasing the bias current of the differential pair, as shown in Fig. 8. But, the bias current has to be as low as possible, since the power consumption has to be low.

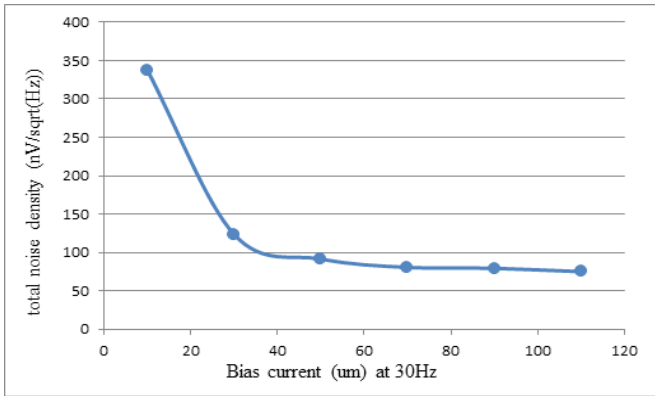


Fig. 8: total noise density (nV/sqrt(Hz) VS bias current (um) at 30Hz

4) *Rail-to-rail opamp – Transistor scaling*

A rail-to-rail op-amp was studied too. The two circuits were the same, except for the differential pairs and the current sources that were used to bias them. The input stage of the rail-to-rail op-amp is shown below (Fig. 9).

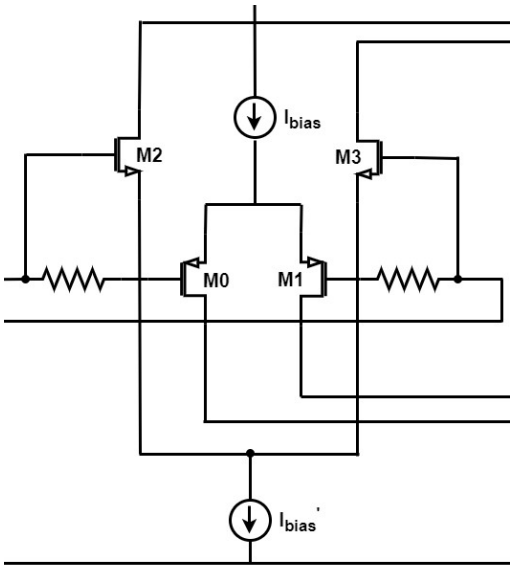


Fig. 9: input stage of the rail-to-rail op-amp

The same process as before was followed. The transistors with the most noise contribution were the M2 and M3 of the nmos differential pair. Then there were the transistors M8 and M9 and with lower noise contribution, there were the M6 and M7. The pmos differential pair had negligible noise contribution, unlike before.

A parameter α was used again, this time for the width and length of the nmos differential pair.

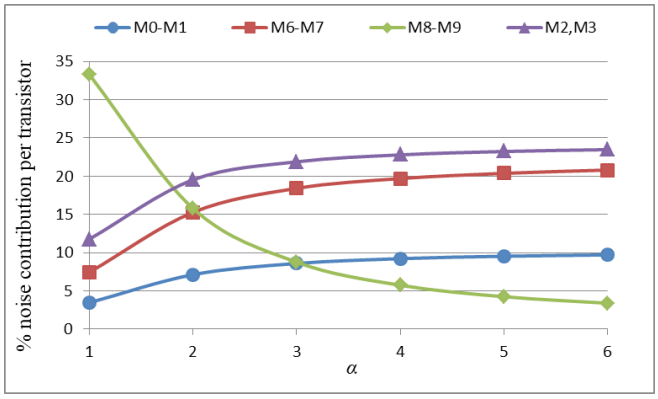


Fig. 10: % noise contribution per transistor pair VS α parameter

As shown in Fig. 10, the nmos differential pair (M2,M3) has 70% of the total noise when α=1. For higher *WL* of M2 and M3, their noise contribution is decreasing while the contribution of the other transistors increases. With the same logic, we change the dimensions of the other transistors that contribute to noise. Also, noise contribution was decreased by increasing the fingers of the MOSFETs with higher contributions.

IV. Finalized Designs and Comparison

In Table II below, these are the dimensions of the transistors that were selected, during the noise optimization. All the other transistors remained with their original dimensions shown in Table I, since they didn't contribute to total noise.

TABLE II. Op-amp MOS Dimensions Post-Optimization - Comparison

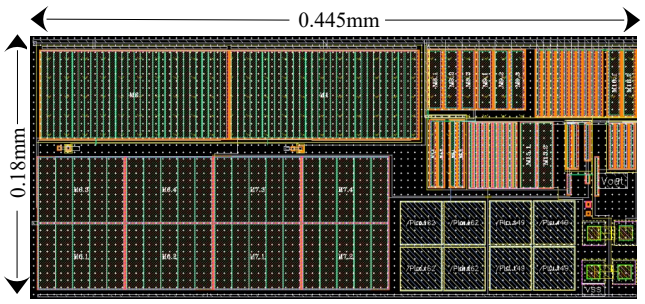
Transistor	**pmos**		**rail-to-rail**	
	W/L	***Fingers***	***W/L***	***Fingers***
M0, M1	60um/4um	30	30um/2um	10
M2, M3	-	-	120um/12um	30
M6, M7	180um/12um	5	90um/6um	1
M8, M9	120um/8um	1	120um/8um	1

Table III includes the final values of some performance parameters of the two op-amps. Both op-amps have low power consumption (1 mW), as expected, and exhibit roughly the same voltage noise when the silicon area of the rail-to-rail op-amp is roughly twice that of the silicon area of the pmos op-amp. Furthermore, the rail-to-rail opamp has a higher gain bandwidth product than the pmos opamp, but the opamp will operate in low frequencies.

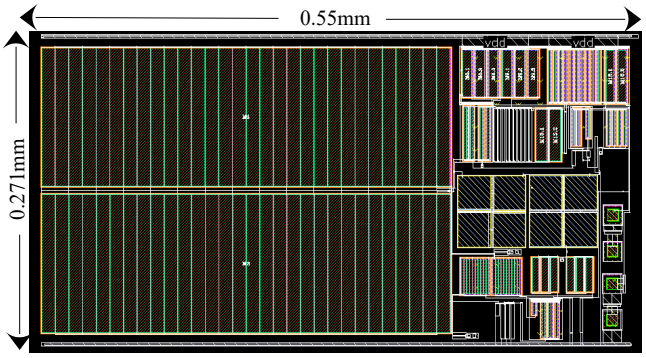
TABLE III. Comparison of pmos and Rail-to-Rail Op-amp

Performance parameters	**pmos**	**rail-to-rail**	**unit**
Input noise at 100Hz	32	33	nV/sqrt(Hz)
Input noise at 1kHz	16.2	15.1	nV/sqrt(Hz)
Gain Bandwidth Product	1.37	5.8	MHz
Power consumption	0.27	0.21	mW
Area	0.08	0.15	mm^2

So, the pmos op-amp, due to its lower silicon area, is preferred. In Fig. 11, the layouts of the two op-amps are shown, with the area of the rail-to-rail op-amp being way larger than the other. The rail to rail design has a layout foorprint equat to 550 um x 271 um occupying 0.15 mm^2 active silicon area, while the non rail to rail design has a layout foorprint equal to 445 um x 180 um occupying 0.8 um^2 active silicon area, value way lower compared to the rail to rail one.

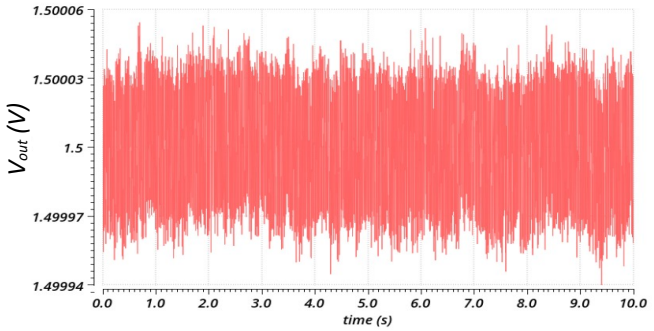


(a)



(b)

Fig. 11: layout of (a) pmos op-amp, (b) rail-to-rail op-amp



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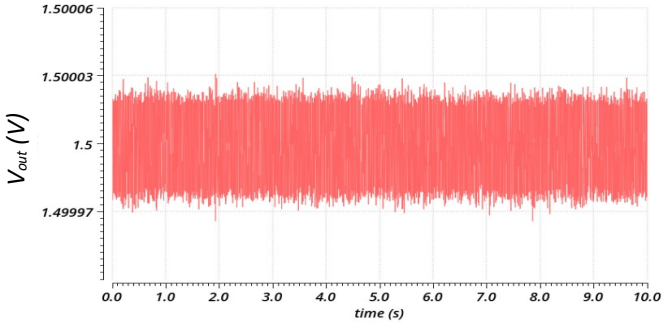

(b)

Fig. 12: Transient noise analysis of pmos op-amp a) pre-optimization, b) post-optimization

Fig. 12 shows the results of transient noise analyses before pre-optimization and post-optimization of the pmos op-amp. After the optimization, there is a significant reduction in the noise, a little higher than 85%.

V. Simulations and Performance

Finally, simulations were performed to evaluate the operation of the pmos opamp, as an I/V converter (transimpedance amplifier) in the electric field mill sensor interface. The current of the field mill sensor, which is passed through the amplifier, ensues from functions (2) and (3).

For the simulations, a sensor with dimensions R=74mm and r=30mm, and with a number of vanes equal to n=2, was examined. The electric field was considered equal to 10kV/m.

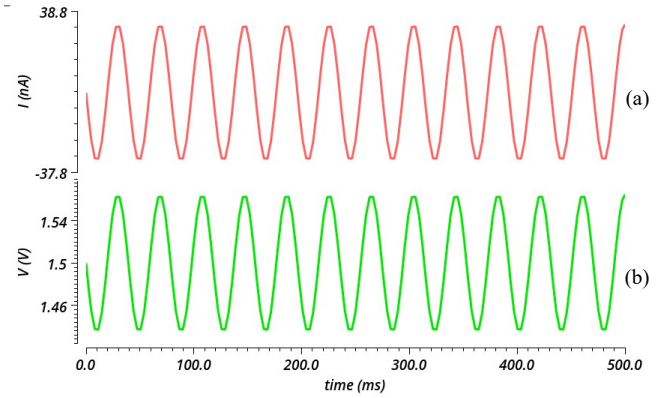

Figure 13: Waveforms of a) I(t) from the sensor that is converted by the transimpedance amplifier b) to V(t)

Fig. 13 shows the operation of the opamp as an I/V converter. For a sinusoidal current from the sensor, a sinusoidal voltage is generated in the output of the opamp.

Also, a parametric analysis was performed, observing the output voltage V(t) of the opamp by changing the value of the electric field from 0 kV/m to 20 kV/m. The peak voltage, V_{peak} of some values of the electric field was measured.

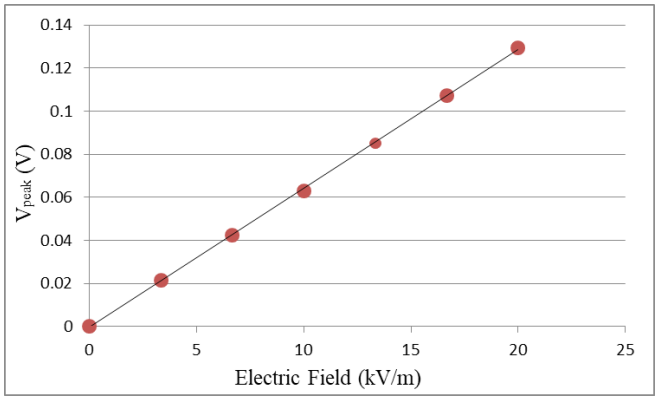

Figure 14: Electric field (kV/m) versus V_{peak} (V)

Fig. 14 shows the proportional dependence of the amplitude of the voltage waveform in the output of the opamp, with the variation of the Electric Field.

VI. Conclusions

Two 3V folded cascode operational amplifiers with low power were compared, in order to select the most suitable one for the preamplification stage of an electric field mill sensor. The first op-amp has a pmos differential pair, while the other is a rail-to-rail one. The significant source of noise is the flicker noise at the low frequencies (100Hz) where the op-amp operates. Due to the requirement for low noise, an advanced noise optimization methodology is presented. Based on the presented noise analysis, it is defined which transistors had the highest noise contribution. The minimization of the total noise requires the increase of the area of these transistors.. By decreasing the input noise, the silicon area is increased. It is concluded that after the noise optimization of both op-amps, the pmos op-amp can have half of the silicon area of the rail-to-rail op-amp, while exhibiting similar noise performance. The presented analysis can be used as a guide for optimizing low frequency preamplification applications in the range of tens of Hz, in terms of noise performance and silicon to cost area trade off.

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