A Hardware-Friendly Low-Power Area-Efficient GMM-Based Analog Classifier For Skin Detection

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***Abstract*—Skin detection is the process of identifying skin pixels in a 2-D image or video. It is a vital part of today's Computer Vision technology and widely spread among applications including medical diagnosis, cryptographic protection, localization tasks and human-machine interaction. To this end, this work proposes a novel, low power ($31-35$nW), low voltage (0.6V), area-efficient ($2098\mu m^2$), GMM-Based analog classifier for skin detection. The architecture consists of bump circuits and a Lazzaro Winner-Take-All circuit. The presented classifier was designed and simulated in a TSMC 90nm CMOS process, using the Cadence IC Suite. To verify the proper operation of the proposed design, a real-world skin segmentation dataset is used. To confirm the circuit's accuracy, post-layout simulation results were compared to a software-based implementation.**

***Index Terms*—Analog VLSI implementation, Area-Efficiency, GMM-Based Classifier, Low-Power design, Skin Detection**

I. Introduction

Nowadays, Internet of Things (IoT) devices become increasingly popular in diverse applications [1]. The backbone of these applications is sensors and actuators, such as cameras, colour and light sensors. A rising research topic in IoT domain is Computer Vision, in which information is extracted from images and videos [2]. There are various methods in which machines are able to process their surroundings, which may include objects, weather conditions or even people. That being said, a pivotal and demanding field in Computer Vision is skin detection [3].

Skin detection has a paramount role in a wide range of applications [4]. This includes computer human interaction, medical diagnosis or assistingly in more complex systems. Human computer interaction benefits from skin detection by enabling computers to identify humans. This is a especially useful for human tracking, identifying hand gestures in sign language or human-machine collaboration. In medical diagnosis, skin detection can be applied in detecting skin cancer (e.g. Melanoma). Furthermore, skin detection methods can be utilized in more complex systems; cryptographic protection methods, like steganography, localization tasks (e.g. in face recognition) or as a segmentation method in media featuring humans.

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All these related applications are in many cases implemented by battery and area depended devices [5]. Due to this fact, new computing paradigms have been introduced. Combining edge [6] and analog computing [7] is a promising solution since the information processing takes place closer to the source (away from data centers), thus minimizing the energy needed for data transferring. This combined with subthreshold techniques results in more power efficient systems [8]. Given the wide range of skin detection applications and motivated by their increased computation requirements, we propose an ultra low power, area efficient analog classifier for general purpose skin detection. The classifier is designed in TSMC 90nm CMOS process and tested in a real-world skin segmentation dataset, compared with a software based implementation.

The remainder of this paper is organized as follows. The background regarding ML-based skin detection and the proposed hardware friendly modification of the GMM-based classifier are explained in Section II. In Section III, the main building blocks and the proposed architecture are presented. A real-world skin detection dataset is used to confirm the proper operation of the proposed classifier in Section IV. A comparison between hardware and software implementation and sensitivity tests are also provided. Some concluding remarks are given in Section V.

II. Background

A. Skin Detection

Skin detection aims to successfully separate a skin pixel from a non-skin one [9]. To this end, various algorithms have been proposed that are primarily divided into two groups; thresholding and ML algorithms [10]. The first use an explicit and fixed boundary, which is in fact a benchmark to categorize each pixel. This is a simple and intuitive method but depends on adequate tuning in order to yield sufficient results. The latter use a training set to build a predictive model, for instance a Bayesian classifier, a binary logistic regression model, a histogram-based model, a neuro-fuzzy inference system etc.

Regardless of the followed method, all algorithms share a common ground. The first step is the selection of a colour code appropriate for pixel segregation and secondly, they all classify each pixel of the given image individually and independently

of its neighbouring pixels. Some colour codes, commonly used in digital image processing, are the RGB (Red-Green-Blue), YC_bC_r (Luminance-Red difference-Blue difference-Red) and HSV (Hue-Saturation-Value) [11]. While the RGB (Red-Green-Blue component) colour code is by far the most used and well-known in digital image processing applications, the YC_bC_r and the HSV codes yield better results. This is mainly due to RGB code failing to explicitly describe the brightness of said pixel, resulting in classification inaccuracies during different lighting conditions.

Opposing to this shortcoming, the YC_bC_r and the HSV codes separate brightness (luminance,Value) from colours. Consequently, the Y or V component of each pixel can be neglected, serving a dual purpose; it minimizes hardware requirements and the skin classification becomes almost invariant of the lighting conditions. Interestingly enough, combining different colour spaces increases the accuracy of the detector. However, this technique results in increased hardware requirements and processing times.

B. Hardware Friendly Modification of GMM-Based Model

In a typical GMM-based classifier [12], the probability of a class being the winning one, given an input vector X, is calculated as:

$$p(C_n|X) = \frac{p(C_n)}{p(X)} \sum_{k=1}^{K^{(n)}} w_k^{(n)} \mathcal{N}(X|M_k^{(n)}, \Sigma_k^{(n)}). \quad (1)$$

Here, $[n]_1^N$ is the index of the class, N is the number of classes, $p(C_n)$ is the prior probability of the class n, $p(X)$ is the evidence probability of the input X, $K^{(n)}$ is a hyperparameter indicating the number of subcategories in a class. The $w_k^{(n)}$, $M_k^{(n)}$ and $\Sigma_k^{(n)}$ are the weight and the mean value and the covariance matrices that describe the multivariate Gaussian function belonging to class n and subcategory k. The index (y) of the winning class is indicated as:

$$y = \underset{n\in[1,N]}{\text{argmax}}\{p(C_n|X)\}. \quad (2)$$

The Hardware friendly implementation is applied when only two classes are considered. In that case, the probability of only one class (C_1) is calculated and compared to a hyperparameter threshold value (I_{th}) [3] to indicate the winning class as in:

$$y = \begin{cases} 1 & \text{if } p(C_1|X) \geq I_{th} \\ 2 & \text{if } p(C_1|X) < I_{th} \end{cases}. \quad (3)$$

In practice, this modification halves the power and area requirements of the classifier.

III. Proposed Architecture

In this Section the analog, hardware-friendly topology of a GMM-based classifier is presented. This architecture requires a single multivariate Gaussian function circuit [13] and a simple Winner-Take-All (WTA) circuit [14]. All transistors operate in the sub-threshold region and the supply voltages are set to $V_{DD} = -V_{SS} = 0.3V$.

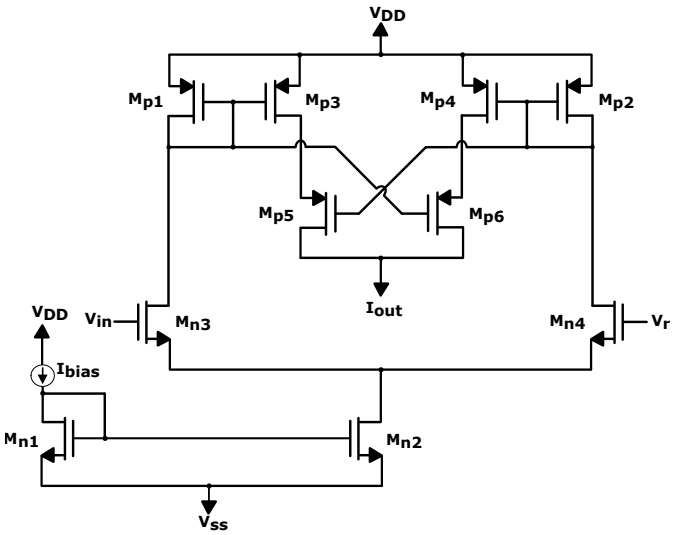

Fig. 1: NMOS differential pair based Bump circuit. The bias current I_{bias} and the voltage parameter V_r control the height and the mean value of the produced Gaussian curve (I_{out}), respectively. The PMOS variant is built accordingly (shown in Fig. 2).

An univariate Gaussian function circuit produces a single output current that represents a Gaussian function [13]. A NMOS differential pair based Bump circuit (NMOS-Bump) is shown in Fig. 1 and its transistors' dimensions are summarized in Table I. By utilizing Bump circuits the process of deriving a multivariate Gaussian is simplified. In particular, the cascaded connection of Bump circuits; biasing each Bump circuit with the output current of the previous one, realizes a multivariate Gaussian function circuit [15], [16]. In this work, the area efficiency of this topology is enhanced by alternatively using the NMOS and PMOS based variations of the Bump circuit. By doing so, the current mirror of a Bump circuit can be ignored as depicted in Fig. 2.

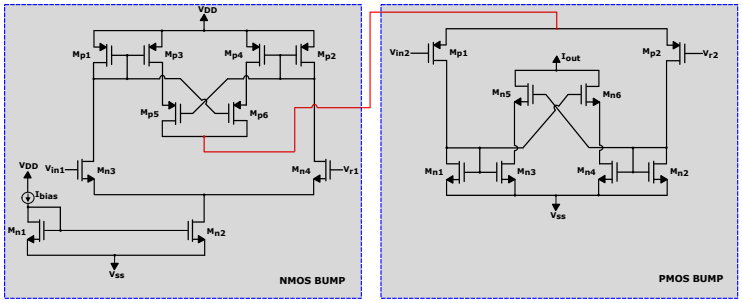

Fig. 2: A 2-D Bump circuit built by sequentially connecting two 1-D Bump circuits. The PMOS current mirror of the second Bump circuit is removed.

TABLE I: MOS Transistors' Dimensions (Fig. 1).

Block	W/L (µm/µm)	Current Correlator	W/L (µm/µm)
M_{n1}-M_{n2}	0.4/4.8	M_{p1}-M_{p2}	1.6/1.6
M_{n3}-M_{n4}	0.4/0.4	M_{p3}-M_{p6}	0.8/1.6

A 2-input WTA circuit is required to extract the final decision by indicating the highest among two input currents [14]. This is achieved through the WTA's two output currents that are in binary format. Specifically, the output current that corresponds to the highest input one has a logical high value, whereas the other has logical low value. This topology is presented in Fig. 3, in which all transistors' dimensions are set as $W/L = 0.4\mu m/1.6\mu m$.

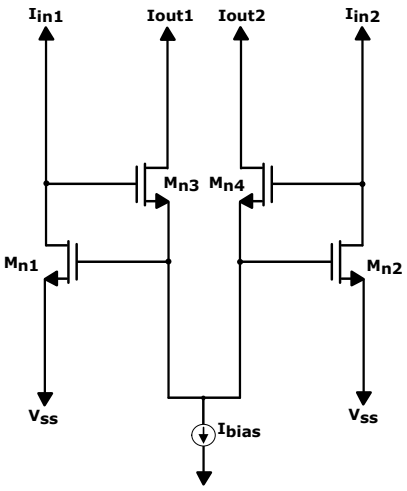

Fig. 3: A 2 input Lazzaro WTA circuit. Its operation is identical to a comparator.

The proposed classifier is designed for a 2-classes and 2-features classification problem, but is scalable regarding the input features. Following the hardware-friendly modification, proposed in Section II, only the probability of 1 class is calculated. The current representing this probability is compared to a constant threshold current using the WTA circuit. The value of this thershold current directly affects the decision boundary of the classifier. Its architecture is presented in Fig. 4.

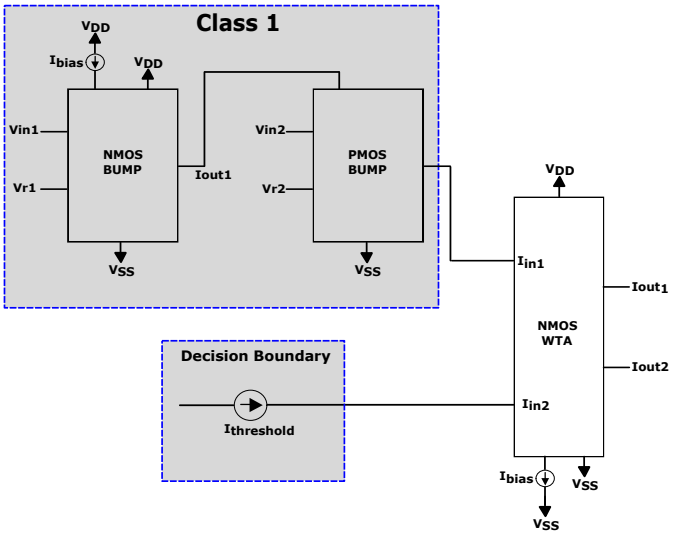

Fig. 4: The proposed Analog GMM-based classifier. (left) Multivariate Bump circuit and Decision Boundary current (right) WTA circuit.

IV. Skin Detection Example and Simulation Results

A real-world skin segmentation dataset is used in order to validate the proper operation of the proposed classifier [17]. In particular, the database was created by University of Texas at Dallas (Productive Aging Laboratory). It consists of RGB values from faces images of diversity of age, gender, and race people. From the dataset, the RGB features were converted to YC_bC_r. In literature, it is a common practice to remove the Y (or V) feature in skin detection problems [11]. The 2 remaining features are used to train and validate the classifier.

Two separate tests are executed in a TSMC $90nm$ CMOS process using the Cadence IC suite, in order to verify the proper operation of the proposed classifier. Both tests were conducted on the layout, which is presented in Fig. 5. The first test compares the hardware and software implementations in terms of classification accuracy. As shown in Fig. 6 and 7 , in which 20 different training test iterations are presented, the post-layout simulation results are highly accurate (summarized in Table II). To confirm the sensitivity of the proposed architecture a Monte Carlo analysis for $N = 200$ points was conducted (the used features were C_bC_r). The Monte Calro histogram, shown in Fig. 8, has a mean value of $\mu_M = 0.91$ and a standard deviation of $\sigma_M = 0.11$.

To further illustrate the performance of the presented classifier, 3 extra architectures were designed and simulated. More specifically, $Case\ 1$ and $Case\ 2$ is the proposed architecture (shown in Fig. 4) for HS and C_bC_r features respectively, $Case\ 3$ is a two-class one-cluster C_bC_r GMM classifier [16], $Case\ 4$ is the same architecture as the first one but with one extra feature (Y) and $Case\ 5$ is exactly the same as the former one, but with RGB features. The simulations result of the 4 architectures are summarized in Table III.

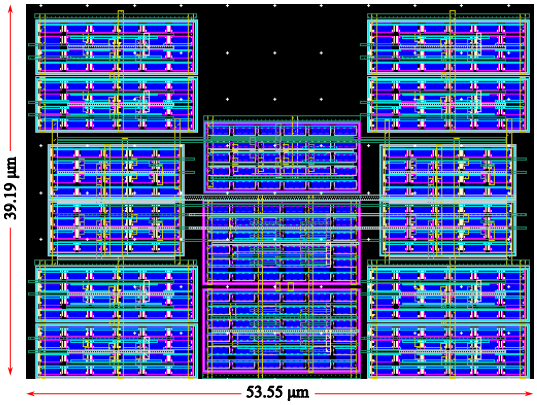

Fig. 5: Proposed Classifier's Layout.

V. Conclusion

A hardware-friendly analog GMM-based implementation was introduced in this work, as a low-power ($31-35$ nW) and area-efficient ($2098\mu m^2$) skin detection circuit. The design methodology which was followed, is based on miniaturization

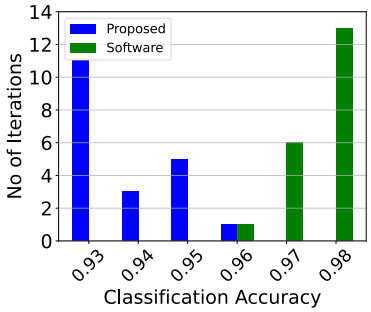

Fig. 6: Comparison between hardware (post-layout simulation) and software implementations over 20 iterations for the proposed classifier, for C_bC_r.

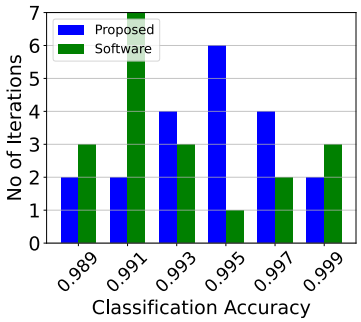

Fig. 7: Comparison between hardware (post-layout simulation) and software implementations over 20 iterations for the proposed classifier, for HS.

TABLE II: Accuracy Results (over 20 iterations).

Method	Best	Worst	Mean	Std.
Software (HS)	0.998	0.988	0.993	0.003
Proposed (HS)	1.0	0.990	0.995	0.003
Software (C_bC_r)	0.983	0.963	0.974	0.006
Proposed (C_bC_r)	0.960	0.928	0.940	0.009

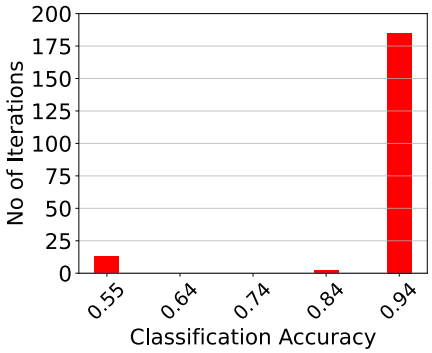

Fig. 8: Post-layout Monte Carlo sensitivity analysis histogram for $N = 200$ points.

and sub-threshold region techniques. The classifier's components are Bump and WTA circuits. Since it has a high accuracy and appropriate sensitivity, it can be used as the main building block in face recognition systems. To confirm the proper operation of the proposed architecture post-layout simulation results are conducted in a TSMC 90nm CMOS process, using a skin segmentation dataset.

TABLE III: Performance Summary

Architecture	Software Accuracy	Hardware Accuracy	Power Consumption	No. of Transistors
Case 1	**0.993**	**0.994**	**31nW**	**22**
Case 2	**0.974**	**0.940**	**35nW**	**22**
Case 3	0.979	0.925	$78nW$	40
Case 4	0.981	0.954	$56nW$	30
Case 5	0.666	0.621	$50nW$	30

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