Buck-Boost Charge Pump based DC-DC converter

Evi Keramida
Department of Electrical and Computer Engineering
University of Thessaly
Volos, Greece
pakerami@uth.gr

George Souliotis
Department of Electrical and Computer Engineering
University of the Peloponnese
Patras, Greece
https://orcid.org/0000-0001-5705-0779

Spyridon Vlassis
Electronics Laboratory, Department of Physics
University of Patras
Patras, Greece
svlassis@physics.upatras.gr

Fotis Plessas
Department of Electrical and Computer Engineering
University of Thessaly
Volos, Greece
fplessas@e-ce.uth.gr

***Abstract*— A dual mode buck-boost charge pump is presented in this paper. The two modes, buck and boost, of the CP can be used by the same circuit for degrading or elevating the output voltage, respectively, compared to the input. Each mode can be achieved by switching only the input-output connections without any other change in the design of the DC-DC converter. This dual mode configuration aims to merge two different functions into one circuit minimizing the area the DC-DC converter occupies on the die. The proposed buck-boost CP has been designed using TSMC 130nm complementary metal-oxide-semiconductor (CMOS) technology providing a 3.3V output voltage from a 2.2V supply voltage when the DC-DC converter operates in boost mode and a 1.6V output voltage from a 3.3V supply voltage in buck mode. A 2uF capacitor has been placed at the output of the CP. For the buck mode, the capacitor of the output must be pre-charged in order for the CP to operate properly.**

Keywords—charge pump, switched capacitor converter, buck-boost charge pump, DC-DC converter, CMOS technology, power management

I. INTRODUCTION

Applications based on the Internet of Things (IoT) and wearable devices are of widespread usage nowadays creating the necessity to minimize the size of ICs and increase the efficiency of the system. The operation of these devices is usually based on the energy taken from the environment which then is converted into power in order that the IC individual components be functional. Many times, the harvested energy is not enough to create the required voltage level and so an additional power management system is needed to transform this energy into the correct voltage value. Charge Pumps (CPs) play a major role in this process as they are simple to implement, can be fully integrated, and occupy small space on the chip. So, they are a good choice as DC-DC converters in low power applications, replacing the linear voltage regulators (LDOs) which formed a common solution in power conversion in the past.

A family of switched capacitor DC-DC converters use CPs to transfer charge through capacitors in order to step up or step down the input to output voltage, operating with the aid of clocked circuits. Many architectures of CPs have been developed over the years and can be found through the literature such as Dickson CP which is the most famous topology because of its simple implementation. Dickson CP is an N-stage architecture consisting of switches and capacitors initially proposed and patented by Dickson, J.F. [1] in 1976. Diode connected transistors are used to transfer charge through the capacitors from stage to stage as shown in Fig.1. Capacitors charge and discharge in between the clock circles, stepping up the voltage from one stage to the next one. The final output voltage depends on the total number of stages, used in this architecture.

Main problem of Dickson's topology is that it lacks efficiency due to mosfets threshold voltage drop. Many other variations of Dickson CP topology have been proposed since then, such as charge transfer switch (CTS) CP, static and dynamic [2], [3] and techniques like gate biasing technique [4], [5] and body biasing technique [6], [7]. These topologies have been developed to overcome the threshold voltage drop problem. Another modification has been proposed by Pelliconi [8] and it is shown in Fig. 2. This topology uses low voltage transistors and a two-phase clock, usually referred to as cross-coupled or latched CP. The proposed CP is a voltage doubler where each stage is realized with standard transistors, and it is driven by a simple two-phase clocking scheme while no specific output stage is needed. The topology consists of two nmos and two pmos transistors operating in two phases by charging and discharging the flying capacitors in every cycle due to the anti-phase and complimentary clocks.

The proposed buck-boost converter is based on Pelliconi's boost CP topology, offers simple design, reduced size, and high conversion efficiency levels. First, we expand the topology and prove that with minor modifications it can support the buck mode also. A theoretical explanation is given. Then we combine the two functions and propose a novel buck-boost converter. The two modes are realized by only switching the external connections of the CP. When the CP operates in boost mode receives a 2.2V voltage at the input and converts it into a 3.3V output voltage. Accordingly, when the CP functions in buck mode it gets a 3.3V voltage at the input and converts it into a 1.6V output voltage.

The present paper is organized in sections as follows: in Section II the architecture of the proposed buck-boost DC-DC converter is described by analyzing the individual blocks of the design. In Section III measurements and results are presented for the dual mode DC-DC converter operating in each mode and finally, in Section IV the paper conclusions are given.

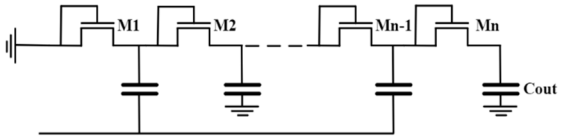


Fig. 1.N-stages Basic Dickson CP

979-8-3503-9958-5/22/$31.00 ©2022 IEEE

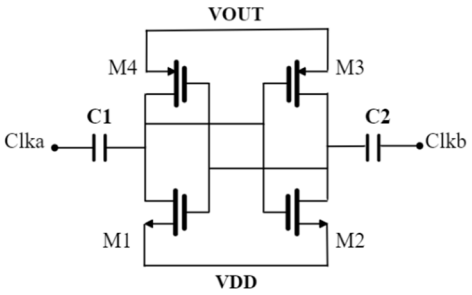


Fig. 2. Architecture of the cross coupled CP

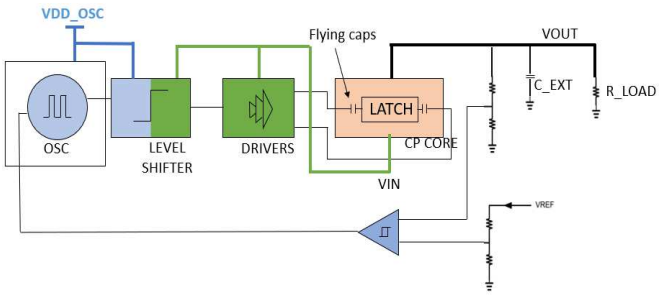


Fig. 3. Proposed Buck-Boost DC-DC converter

II. CIRCUIT ARCHITECTURE

The proposed architecture of the buck-boost DC-DC converter is shown in Fig. 3. The converter consists of an oscillator (OSC) with a 100MHz operating frequency, a level shifter, a comparator, a suitable number of pre-drivers and drivers, and finally the core of CP. The internal two flying capacitors are 150pF each. The size of pumping capacitors depends on the switching frequency and decreases as the switching frequency increases reducing that way the area the CP occupies and improving the power efficiency simultaneously. Albeit it should be mentioned that higher frequency leads to more losses due to parasitic elements. So, the value of the capacitors is chosen by the tradeoff between capacitor area, frequency and losses due to parasitic elements. The initial size of the flying capacitors can be determined by the desirable output current and the switching frequency using (1):

$$Iout = C\frac{dV}{dT} \qquad (1)$$

However, the final value of the pumping capacitors is determined though simulations as they affect the efficiency of the CP. Power efficiency also depends on the consumption of the individual blocks, like the oscillator, the level shifters, the drivers and the comparator.

Two supply voltages are needed in order for the DC-DC converter to operate in both modes, one for the oscillator and one for the CP core. The oscillator's supply voltage is 1V. Core's supply voltage is 2.2V for the boost mode and 3.3V for the buck mode.

A. Oscillator

A conventional ring oscillator is used to produce the required clock for the switches. The ring oscillator consists of three delay cells in a closed loop. Each delay cell has three inverters connected in series. The combination of the number of the employed delay cells with the number of the inverters inside of them adjusts the oscillator frequency. As shown in Fig.4, the ring oscillator topology that has been selected has a simple design and offers a wide tuning range and low power consumption. The operating frequency and the oscillator performance in this application are not critical, and therefore this operates as a free-running oscillator. The operating frequency has been chosen at 100MHz with a 1V supply voltage. The absence of capacitors and inductors makes the topology ideal for low power applications, with small layout area.

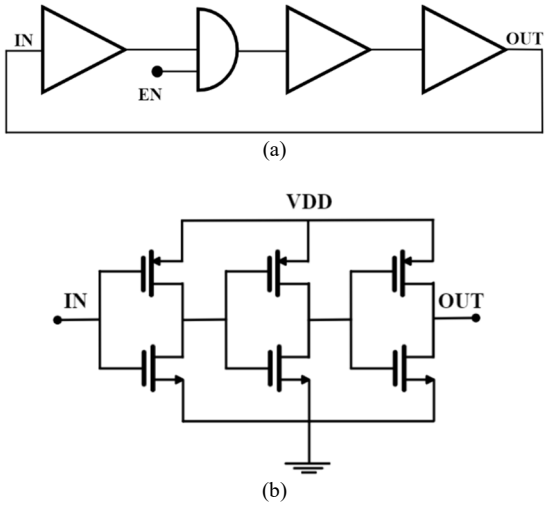


Fig. 4 The ring oscillator circuit: a) block diagram of the oscillator b) the delay cell

B. Comparator

A comparator is employed to compare the output voltage of the CP with the maximum and minimum levels of the required output voltage. When the output voltage is lower than the minimum threshold the comparator activates the oscillator starting the charging process. When the maximum voltage is achieved, the comparator deactivates the oscillator. Due to the load consumption, the output is gradually discharged until the lower threshold, where the charging starts over. In order for the comparator to switch properly between the two thresholds, a comparator with hysteresis has been used.

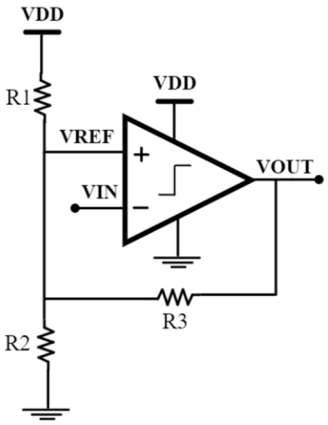


Fig. 5. The comparator with hysteresis topology

C. Level Shifter and Drivers

Level shifters are required to convert the oscillator output to the voltage level needed in the switches of the CP core, as shown in the DC-DC converter topology of Fig. 3. It operates

with two supply voltages, the input one should be the same with the oscillator's supply voltage, and the output with the CP core input (VIN) or output (VOUT) voltage. Thus, the driving voltage of the CP core devices is always at the correct level. More specifically, for the boost mode operation, input supply voltage of the level shifter equals 1V, the oscillator's supply voltage, and the output equals the input supply voltage of the core of CP (VIN) which in this design equals 2.2V. When the buck mode is selected, then again, the input supply voltage of the level shifter equals the oscillator's supply voltage but the output supply terminal is now connected to the output of the CP so the clock has the required amplitude. Drivers need the same voltage supply as the output supply voltage of the level shifter in order to be able to drive the core of the CP properly. In favor of the correct operation of the level shifter, the capacitor at the output of the circuit must be pre-charged to some voltage level, otherwise, the system could not be able to work in the buck mode. In the boost mode, this is not needed.

D. Core of Charge Pump

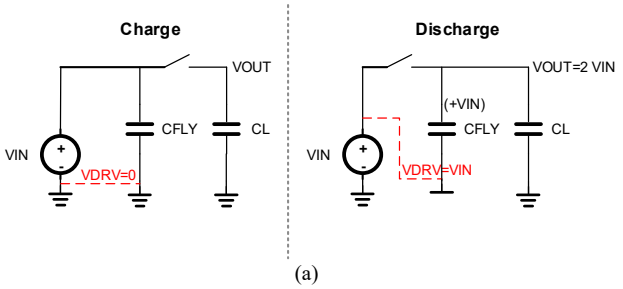
The core of the CP is based on Pelliconi's architecture and the operation of the boost mode is depicted in Fig.6. In the first semi period, CLK is low and $\overline{CLK}$ is high, so M1 and M4 are ON and capacitor C1 is charged to Vin, at the same time C2 which has already been charged in Vin now charges the capacitor of the output which voltage scales up to 2*Vin. During the second semi period, CLK is high and $\overline{CLK}$ is low and the operation of the pumping capacitors is reversed respectively. The output voltage is given by the expression bellow:

$$Vout = Vin + Vcfly = 2Vin \qquad (3)$$

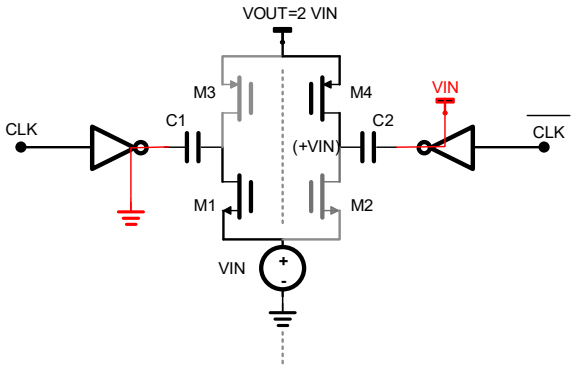
Accordingly for the buck mode the operation is depicted in Fig. 7. In the first semi period, CLK is high and $\overline{CLK}$ is low, so M2 and M3 are ON and capacitor C1 is charged to Vin-Vout and C2 discharges on the output capacitor which voltage now is equal to Vin/2. During the second semi period, CLK is low and $\overline{CLK}$ is high and the operation of the pumping capacitors is reversed respectively. Each of expressions (4) and (5) represent the charging and discharging phase of the buck mode.

$$Vcfly = Vin - Vout \quad (4)$$

$$Vout = Vin/2 \quad (5)$$

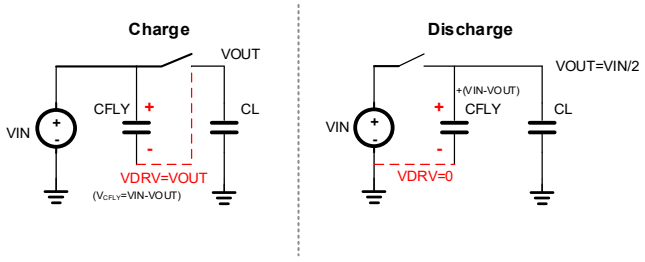


(a)

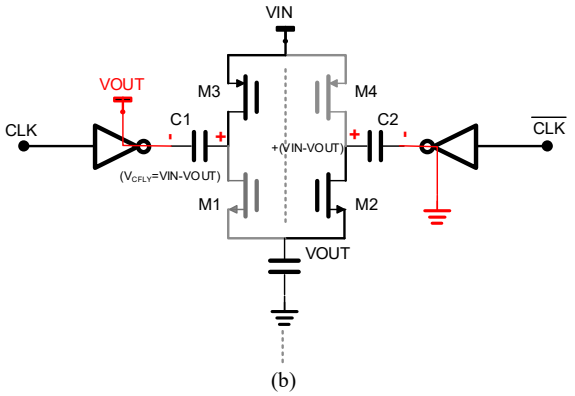


(b)

Fig. 6. Boost Cross Coupled CP (a) charge/discharge and (b) core of CP in boost mode



(a)



(b)

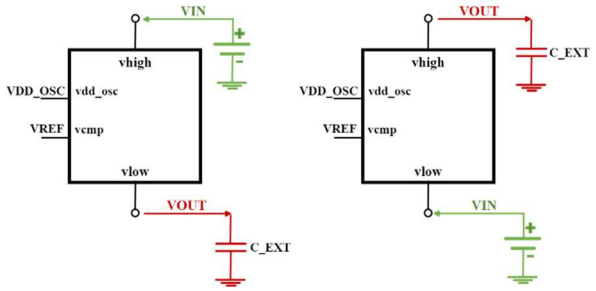
Fig. 7. Buck Cross Coupled CP (a) charge/discharge and (b) core of CP in buck mode

III. PROPOSED BUCK-BOOST CP OPERATION AND VERIFICATION

The proposed buck-boost CP has been designed and simulated in TSMC 130nm technology. In order for the system to operate in each of the two modes, only an interchange of the low voltage (vlow) and high voltage (vhigh) terminals of the CP is needed, as depicted in in Fig. 8a and Fig. 8b. In boost mode the input voltage is connected to vlow and the output of the CP is connected to vhigh. In buck mode these two connections are switched and the input is connected to vhigh and the output is connected to vlow.

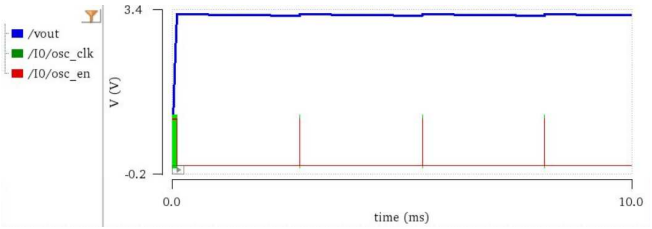
The supply voltage in the boost mode, is 2.2V and the desired output voltage must be equal to 3.3V, with an output capacitive load equal to 2uF. In Fig. 9, the post-layout simulations results are shown for the output voltage, the enable signal and the oscillator output. In Fig. 9a the results are depicted for long operation time, while in Fig. 9b is given a better view during the enable-disable of the oscillator. The PVT corner simulation results are shown in Fig.10. In those simulations a smaller capacitive load has been used to

demonstrate better the transitions between the charging and discharging cycles.

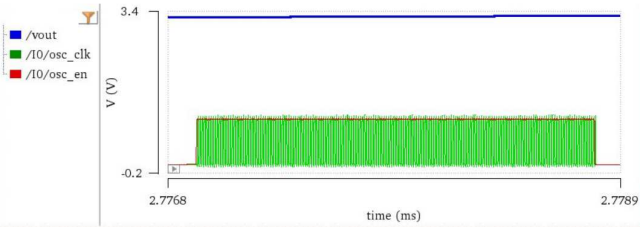


(a) (b)

Fig. 8. External connectivity for a) buck mode and b) boost mode



(a)



(b)

Fig. 9. Postlayout simulation results in boost mode (Vin = 2.2V, Vout = 3.3V, Cext = 2uF) a) DC Output voltage with enabling signal and oscillator output and b) closer view during oscillator activation.

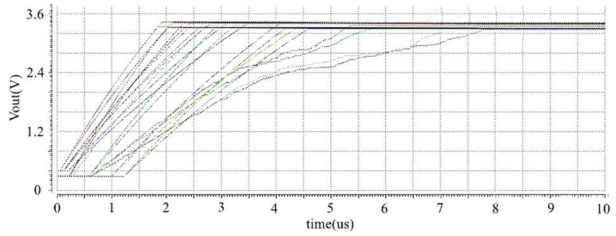
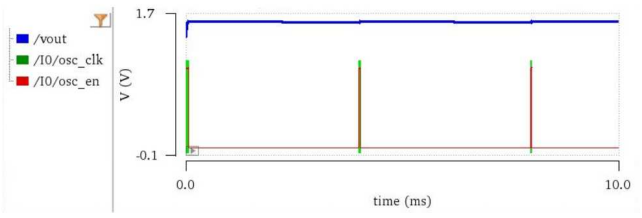
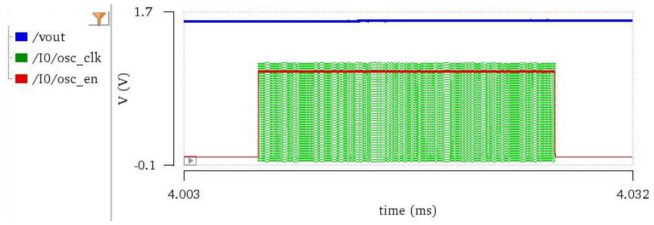


Fig. 10. PVT corners postlayout simulation results in boost mode (Vin = 2.2V, Vout = 3.3V, Cext = 10nF)



(a)



(b)

Fig. 11. Postlayout simulation results in buck mode (Vin = 3.3V, Vout = 1.6V, Cext = 2uF) a) DC Output voltage with enabling signal and oscillator output and b) closer view during oscillator activation.

For the buck mode, the simulated results are shown in Fig. 11. The input voltage is equal to 3.3V and the output is equal to 1.6V. The external capacitor in this mode must be pre-charged in order for the system to be able to step down the input voltage to the desired output voltage level. Finally, the layout of the proposed circuit is depicted in Fig. 12.

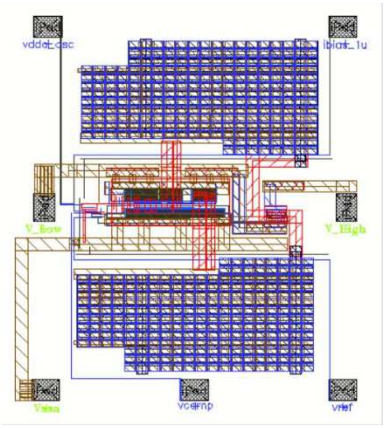


Fig. 12. Layout of the proposed circuit

IV. CONCLUSION

A dual buck-boost charge pump based on Pelliconi's boost charge pump topology, is presented in this paper. We show for the first time that the circuit is able to operate in buck mode also. The proposed design is able to combine two operational modes in one by only switching the high and low voltage connections of the CP. The architecture of the buck-boost CP occupies small area (672.14um x 931.84 um), is fully integrated and easy to implement. The dual mode CP has been design in 130 nm CMOS technology and verified using Cadence Virtuoso tool. Future work should focus on fully evaluating the proposed solution and comparing with previously reported state of the art works.

REFERENCES

[1] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE J. Solid State Circuits, vol. SC-11, pp. 374–378, June 1976

[2] Wu, J.-T.; Chang, K.-L. MOS charge pumps for low-voltage operation. IEEE J. Solid-State Circuits 1998, 33, 592–597

[3] Shiau, M., Hsieh, Z.H., Hsieh, C., Liu, H., & Liu, D. (2007). A Novel Static CTS Charge Pump with Voltage Level Controller for DC-DC Converters. 2007 IEEE Conference on Electron Devices and Solid-State Circuits, 481-484.

[4] D'Arrigo, S.; Imondi, G.; Santin, G.; Gill, M.; Cleavelin, R.; Spagliccia, S.; Tomassetti, E.; Lin, S.; Nguyen, A.; Shah, P.; et al. A 5 V-only 256 kbit CMOS flash EEPROM. In Proceedings of the IEEE International

Solid-State Circuits Conference, 1989 ISSCC, New York, NY, USA, 15–17 February 1989; pp. 132–133.

[5] M. J. Turnquist, G. de Streel, D. Bol, M. Hiienkari and L. Koskinen, "Effects of back-gate bias on switched-capacitor DC-DC converters in UTBB FD-SOI," 2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2014, pp. 1-2, doi: 10.1109/S3S.2014.7028200.

[6] Sawada, K.; Sugawara, Y.; Masui, S. An on-chip high-voltage generator circuit for EEPROMs with a power supply voltage below 2 V. In Proceedings of the Symposium on VLSI Circuits, Kyoto, Japan, 8–10 June 1995; pp. 75–76

[7] N. Cheraghi Shirazi, A. Jannesari, P. Torkzadeh, Self-start-up fully integrated DC-DC step-up converter using body biasing technique for energy harvesting applications, AEU - International Journal of Electronics and Communications,Volume 95,2018,Pages 24-35,ISSN 1434-8411,https://doi.org/10.1016/j.aeue.2018.07.033

[8] Pelliconi, R.; Iezzi, D.; Baroni, A.; Pasotti, M.; and Rolandi, P. “Power efficient charge pump in deep submicron standard CMOS technology,” Solid-State Circuits, IEEE Journal of, vol. 38, no. 6, pp. 1068–1071, 2003