Nano-Watt Voltage References for High Supply Voltages

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***Abstract*—This paper presents two voltage reference circuits that can operate in the supply voltage range of 7-17V and 9-15V while consuming less than 3.5 nA at 17V supply voltage and 8.47 nA at 15V supply voltage. The proposed voltage references consist of only MOSFETs, operated in the subthreshold region since low power consumption is required. The circuits have a mean reference voltage of 2.413V and 2.507V with the best temperature coefficient (TC) being 80 ppm/ºC and 24 ppm/ºC, respectively. The proposed voltage references were designed in XFAB XH018 180nm technology occupying an area of 0.079 mm² and 0.038 mm², respectively.**

Keywords—Voltage reference, nano-watt, high supply voltage, subthreshold, temperature compensation

I. INTRODUCTION

The voltage reference is an essential building block in analog systems such as regulators, DACs (Digital Analog Converters), and ADCs (Analog Digital Converters), to name a few. Depending on the application, references can operate at either high supply voltages or low supply voltages and can consume power ranging from picowatts to milliwatts. High supply voltage references can be employed in power management ICs [1], [2], and in telemetry powering applications [3], [4]. However, most of them are not suitable for nanowatt and picowatt applications since they consume microwatts at best. On the other hand, low supply voltage references operating at nanowatts and picowatts comprise the vast majority of today's references [5]-[9]. These references are appropriate for low power applications, but they cannot work for supply voltages over 5V. There is a nanowatt voltage reference [10] that can operate at maximum supply voltage of 6V.

In this work, two voltage references which consume nanowatts and can operate at supply voltages of 7-17V and 9-15V are presented. The proposed references employ 10V HV NMOS and 15V HV PMOS transistors in order to function at high supply voltages.

The paper is organized as follows. In Section II, the two voltage reference circuits are described. In Section III, the postlayout simulated results are presented, and in Section IV, conclusions are discussed.

II. CIRCUITS DESCRIPTION

A. First Voltage Reference

Fig. 1 illustrates the schematic of the first proposed voltage reference. It consists of a current source circuit (M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{22} and M_{23}) and a temperature compensation circuit (M_1, M_2, M_3, M_4, M_5, M_6, M_7, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20} and M_{21}). Also, cascode transistors are employed for a higher supply voltage and to improve line regulation and PSRR. For low power consumption, all transistors must be operated in the subthreshold region.

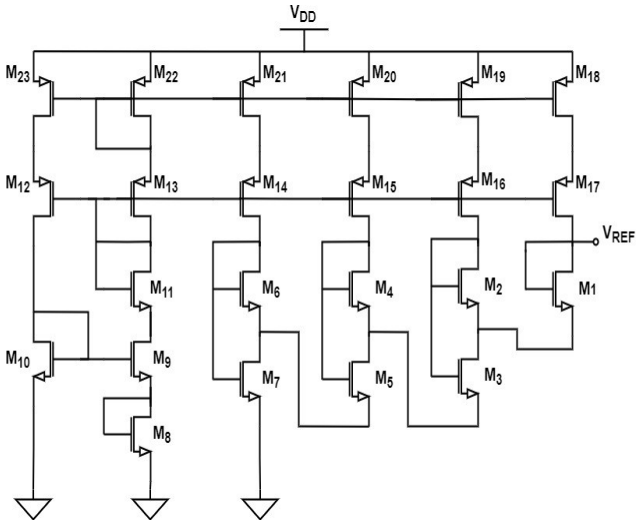

Fig. 1: Schematic of the first voltage reference.

The equation for a MOSFET in subthreshold can be expressed as

$$I_D = KI_0 e^{\frac{V_{GS}-V_{TH}}{mV_T}} \times \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \qquad (1)$$

With $K = W/L$ and $I_0 = \mu C_{ox}(m-1)V^2$ .Where μ is mobility, is C_{ox} oxide capacitance, W is transistor width, L is transistor length, m is subthreshold slope factor ($m = 1 + \frac{C_d}{C_{ox}}$ where C_d is depletion capacitance), $V_T = \frac{kT}{q}$ is thermal voltage, V_{GS} is gate-source voltage, V_{TH} is transistor threshold voltage and V_{DS} is drain-source voltage. For $V_{DS} > 4V_T$, (1) can be rewritten as

$$I_D = KI_0 e^{\frac{V_{GS}-V_{TH}}{mV_T}} \qquad (2)$$

The current source circuit is based on [11] and its principle of operation depends on transistors M_8, M_9, and M_{10}. For these three transistors, and assuming that current I_{BIAS} is equal to all of them, we have, with the help of (2)

$$\begin{aligned} V_{GS10} &= V_{GS9} + V_{GS8} \\ V_{GS9} &= V_{GS10} - V_{GS8} \\ &= mV_T \ln(K_8/K_{10}) \end{aligned} \qquad (3)$$

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Employing again (2) to (3), equation (4) can be rewritten as follows

$$mV_T \ln\left(\frac{I_{BIAS}}{K_9 I_0}\right) + V_{TH9} = mV_T \ln\left(\frac{K_8}{K_{10}}\right)$$
$$I_{BIAS} = K_9 I_0 e^{\ln\left(\frac{K_8}{K_{10}}\right) - \frac{V_{TH9}}{mV_T}} \quad (4)$$

The I_{BIAS} current is delivered to the temperature compensation circuit, which produces the reference voltage. From Fig. 1, the reference voltage V_{REF} is given by

$$V_{REF} = V_{GS1} + V_{DS3} + V_{DS5} + V_{DS7}$$
$$= V_{GS1} + V_{GS3} - V_{GS2} + V_{GS5} \quad (5)$$
$$- V_{GS4} + V_{GS7} - V_{GS6}$$

And as seen before, (3), (5) can be rewritten as

$$V_{REF} = V_{GS1} + mV_T \ln\left(\frac{24K_2K_4K_6}{K_3K_5K_7}\right)$$
$$= V_{TH1} + mV_T \ln\left(\frac{I_{BIAS2}24K_2K_4K_6}{K_1I_0K_3K_5K_7}\right) \quad (6)$$

Where we assumed that the mismatch between the threshold voltages of the transistors can be ignored and all the transistors except M_3, M_5, and M_7 draw the same current. For M_3, M_5 and M_7, we have $2I_{BIAS}$, $3I_{BIAS}$, and $4I_{BIAS}$, respectively. Therefore, equation (6) has two terms that exhibit opposite temperature dependence: thermal voltage V_T, which is proportional to absolute temperature (PTAT), and threshold voltage V_{TH}, which is complementary to absolute temperature (CTAT) [12]. So, for a certain I_{BIAS}, proper sizing of transistors M_1-M_7 can achieve a zero TC at a certain temperature.

B. Second Voltage Reference

Fig. 2 depicts the schematic of the second proposed voltage reference. The reference is biased by the zero-V_{GS} M_1 transistor. This transistor produces a leakage current, which is given by the following equation

$$I_1 = K_1 I_0 e^{\frac{-V_{TH1}}{mV_T}} \quad (7)$$

In figure 2, it is observed that transistors M_6-M_{25} form four differential pairs. As stated in [9], a differential pair can be used to generate a PTAT voltage. So, by adding the PTAT voltage of the differential pairs with the CTAT voltage produced by the diode connected MOSFET M_5 [13], a zero temperature coefficient at a certain temperature can be obtained. Therefore, the reference voltage V_{REF} is expressed as follows

$$V_{REF} = V_{GS5} + V_{SG7} - V_{SG9} + V_{SG12}$$
$$-V_{SG14} + V_{SG17} - V_{SG19} + V_{SG22} - V_{SG24} \quad (8)$$

And as seen before, (3) and (6), (8) can be rewritten as

$$V_{REF} = V_{TH5} + mV_T \ln\left(\frac{I_1K_8K_9K_{13}K_{14}K_{18}K_{19}K_{23}K_{24}}{K_5I_0K_7K_{10}K_{12}K_{15}K_{17}K_{20}K_{22}K_{25}}\right) \quad (9)$$

Where it is considered that the PMOS transistors in the differential pairs have uneven currents because the size of the NMOS in the current mirrors is not the same. Hence, by selecting the proper aspect ratios for the transistors inside the logarithm in (9), a zero temperature coefficient can be accomplished.

III. Postlayout Simulation Results

A. Postlayout Simulations for the First Circuit

The proposed reference was implemented in XFAB XH018 180nm technology. The layout and aspect ratios of the transistors are shown in Fig. 3 and Table I, respectively. The area of the layout is approximately 0.079 mm^2. Fig. 4 depicts the simulation of the voltage reference versus temperature ($-20℃$ to $80℃$) at 17V supply voltage. The circuit was simulated in four extreme conditions, wo, wp, ws, wz, and the corresponding results are displayed in Table II. The TC has a value of 80 ppm/℃ reaching a maximum value of 127 ppm/℃ in the worst power condition, as shown in this table.

Fig. 5 shows the simulation of the reference as a function of temperature for different values of supply voltage, while Fig. 6 illustrates the reference versus the supply voltage at room temperature. The circuit works properly with a supply voltage ranging from 7V to 17V and has a line regulation of 0.53%/V.

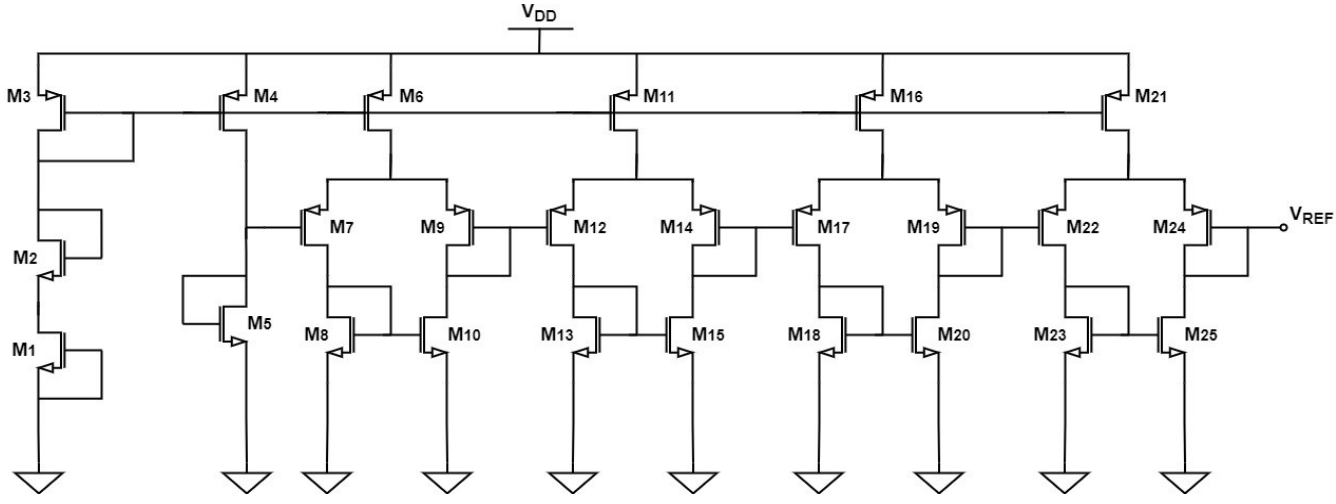

Fig. 2: Schematic of the second voltage reference.

The power supply rejection ration (PSRR) simulation is shown in Fig. 7. The PSRR is −61 dB at 10 Hz and −68 dB at 1 MHz, while dropping to −44 dB at 1 kHz. The current consumption of the circuit is quite low, having a value of 3.47 nA at 17V supply at room temperature and the worst value is only 3.54 nA.

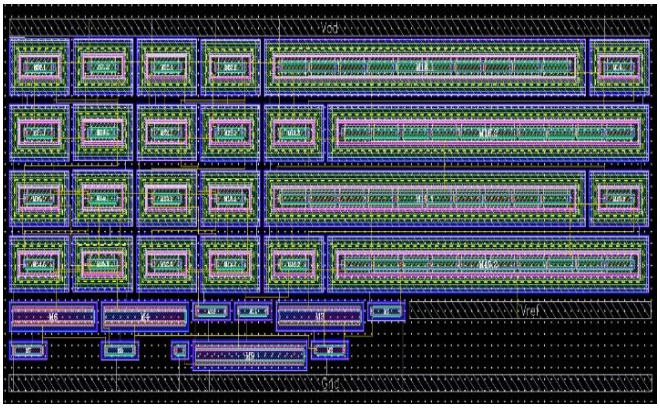

Fig. 3: Layout of the first circuit.

TABLE I ASPECT RATIOS OF THE FIRST CIRCUIT

	W/L	m
M12, M13, M14, M15, M16, M19, M20, M21, M22, M23	2.5/20	2
M1, M3, M5, M7, M10, M11	2.5/20	1
M17, M18	25/20	2
M8	2.5/5	1
M9	80/5	1
M2, M4, M6	60/5	1

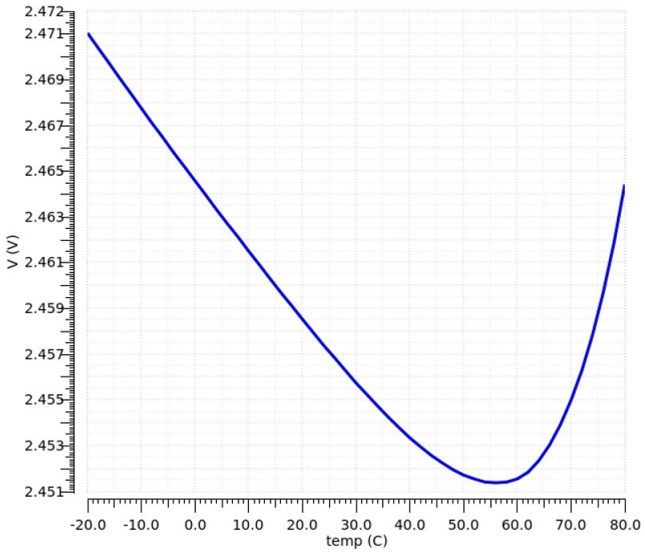

Fig. 4: V_{REF} versus temperature at V_{DD}=17V.

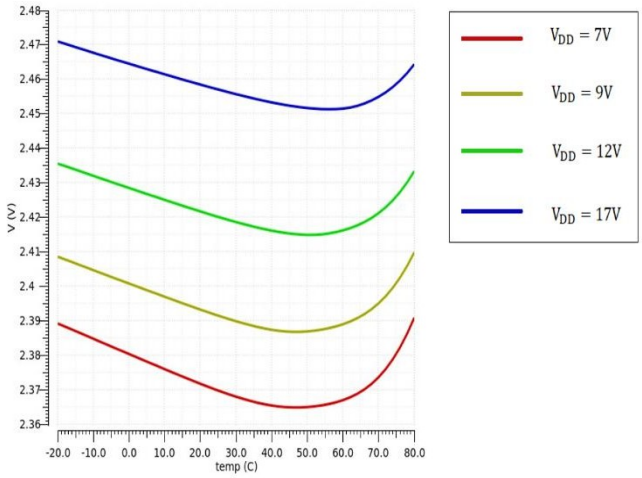

Fig. 5: V_{REF} as a function of temperature at different supply voltages.

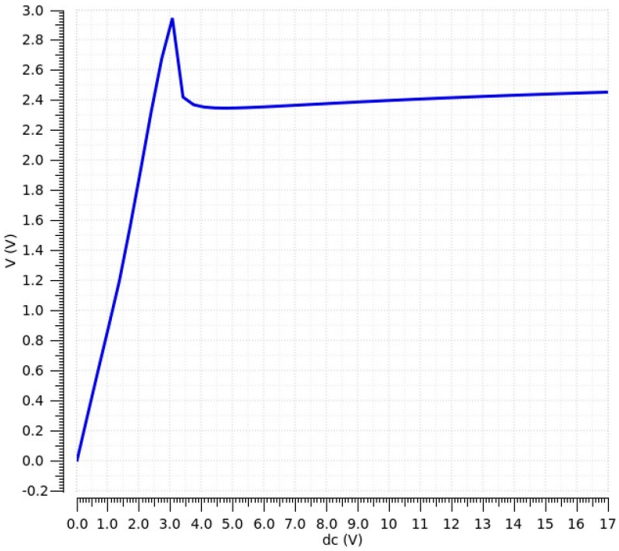

Fig. 6: V_{REF} versus V_{DD} @ 27°C.

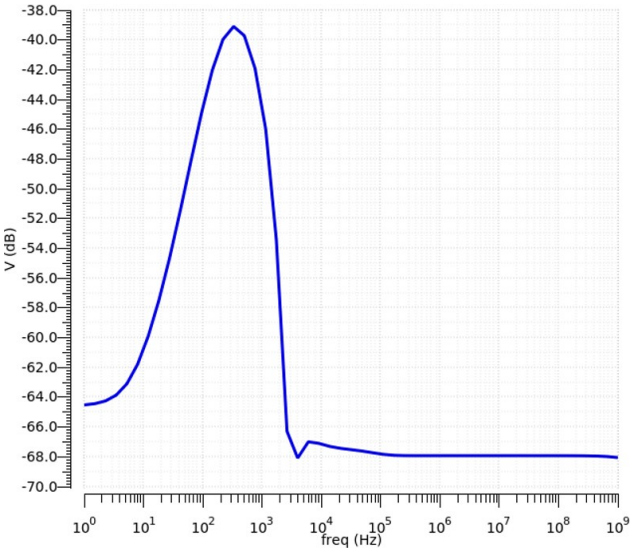

Fig. 7: PSRR of V_{REF} @ 27°C with a 17V supply voltage.

TABLE II CORNER ANALYSIS OF THE FIRST CIRCUIT

	typical	wo	wp	ws	wz
Current Consumption (nA) at room temperature	3.47 @17V	3.43 @17V	3.54 @17V	3.40 @17V	3.51 @17V
TC (ppm/ºC)	80	82	127	66	77
PSRR (dB) **@10Hz** **@1kHz** **@1MHz**	-61 -44 -68	-60 -45 -68	-61 -44 -68	-60 -45 -68	-61 -44 -68
Line Regulation (%/V)	0.37	0.40	0.39	0.35	0.34

B. Postlayout Simulations for the Second Circuit

The second circuit was implemented using the same technology as the first one. The layout is illustrated in Fig. 8 and the aspect ratios of the transistors are displayed in Table III. The area occupied by the layout is approximately 0.038 mm^2.

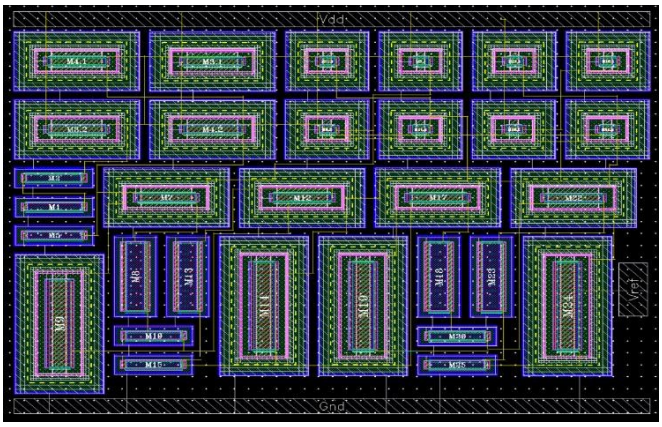

Fig. 8: Layout of the second circuit

TABLE III ASPECT RATIOS OF THE SECOND CIRCUIT

	W/L	m
M1, M2, M5, M7, M10, M12, M15, M17, M20, M22, M25	2.5/20	1
M3, M4	2.5/20	2
M6, M11, M16, M21	2.5/5	2
M8, M13, M18, M23	28/7	1
M9, M14, M19, M24	36/7	1

Fig. 9 depicts the simulation of the voltage reference as a function of temperature (−20℃ to 80℃) at a 15V supply voltage. The TC is 24 ppm/℃ having a worst value of 86 ppm/ºC in worst speed condition, as shown in Table IV. Fig. 10 and Fig. 11 show the supply voltage dependency, where the line regulation from 9 to 15V is 0.4%/V.

Fig. 12 illustrates the PSRR at room temperature with a 15V supply. The PSRR has a value of -63 dB at 10Hz and a value of -81 dB at 1MHz, while dropping to -53 dB at 1kHz.

The current consumption is larger than the first circuit but still low enough, with a value of 8.467 nA at 15V at room temperature while, for the worst power condition, the value is only 9.97 nA.

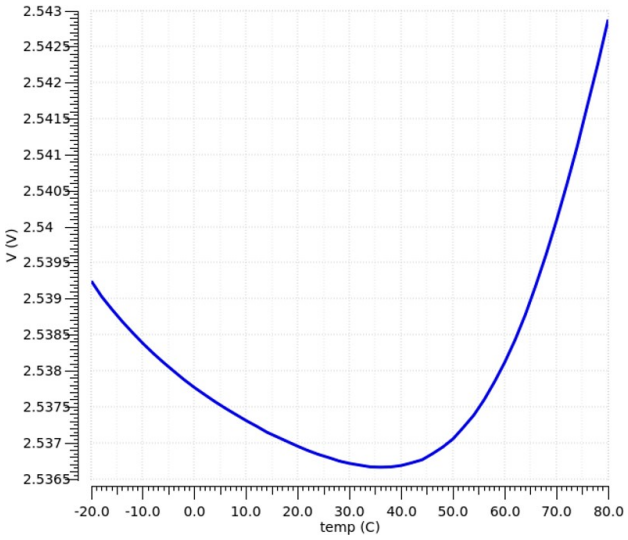

Fig. 9: V_{REF} versus temperature at V_{DD}=15V.

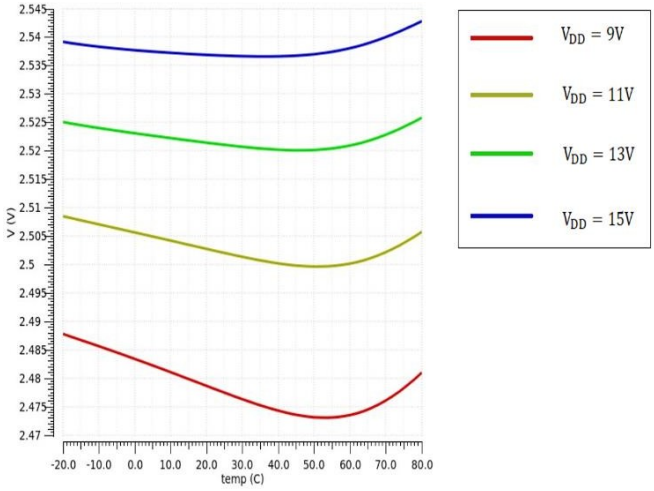

Fig. 10: V_{REF} as a function of temperature at different supply voltages.

TABLE IV CORNER ANALYSIS OF THE SECOND CIRCUIT

	typical	wo	wp	ws	wz
Current Consumption (nA) at room temperature	8.47 @15V	8.31 @15V	9.97 @15V	7.27 @15V	8.62 @15V
TC (ppm/°C)	24	30	68	86	19
PSRR (dB) **@10Hz** **@1kHz** **@1MHz**	 -63 -53 -81	 -63 -53 -81	 -63 -53 -81	 -62 -53 -81	 -63 -53 -81
Line Regulation (%/V)	0.40	0.41	0.39	0.41	0.39

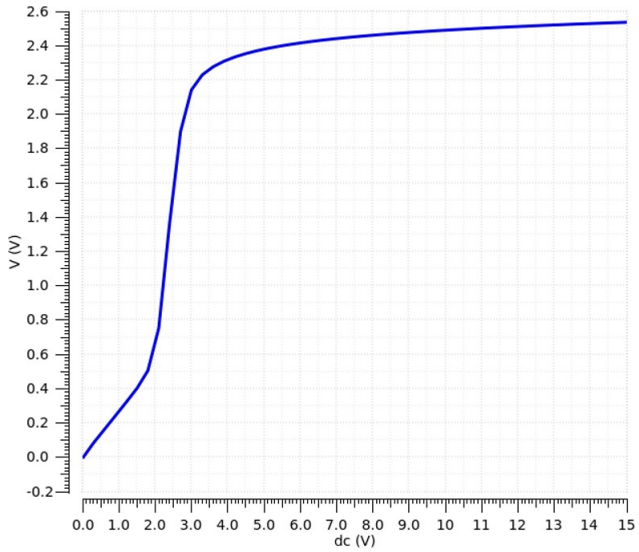

Fig. 11: V_{REF} versus V_{DD} @ 27°C.

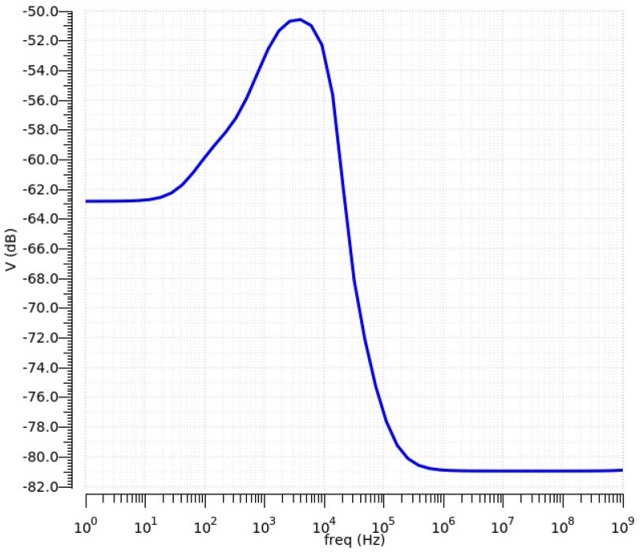

Fig. 12: PSRR of V_{REF} @ 27°C with a 15V supply voltage.

Table V shows the performance comparison of the proposed references with other works. It can be seen that the references that were designed have the lowest power consumption while operating at high supply voltages. Additionally, the supply voltage range is wider than [8], [10], and [14], but not as wide as [15] and the commercial circuit [16]. It is also obvious that the designs in [14], [15], and [16] present much better TC performance in a larger temperature range. However, to achieve this performance, they consume power in the range of μW and mW, which is not acceptable for ultra-low power applications. The work in [8] has a very low TC while consuming nanowatts, but can not operate with a higher than 3V supply. Furthermore, the PSRR of the circuits is worse at lower frequencies compared to [10], but without employing any pre-regulator circuit as in [10], they achieve adequate values. Finally, the second circuit occupies the smallest area among all the designs, except [10].

IV. Conclusion

Two voltage references that employ only MOSFETs and achieve ultra-low power consumption were designed for supply voltages up to 17V. The circuits exhibit a very low current consumption at 3.47 nA and 8.47 nA while operated in the highest supply voltage, so they can be used in general in ultra-low power applications. Also, they present a reference voltage higher than 2V, which makes them suitable for high supply voltage applications.

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TABLE V PERFORMANCE COMPARISON

	First Cir.	Second Cir.	[8]	[10]	[14]	[15]	[16]
Process	0.18 µm	0.18 µm	0.35 µm	0.18 µm	0.35 µm	0.18 µm BCD	XFET
Supply Voltage (V)	7 - 17	9 - 15	1.4 - 3	1.5 - 6	2.6 - 5	3 - 18	3 - 18
Current Consumption (nA) at room temperature	3.47 @17V	8.47 @15V	214.3 @1.4V	42 @1.5V	94000 @N/A	279600 73000 (BGR core) @N/A	3×10^6 @7V
V_{REF} (V)	2.413 (mean)	2.507 (mean)	0.745	0.985	2.47	2.048	2.5
Temperature Range (ºC)	-20 to 80	-20 to 80	-20 to 80	-40 to 85	-60 to 150	-40 to 125	-40 to 125
TC (ppm/ºC)	80	24	7	60.86	3	1.2	3
PSRR (dB)	-61 @10Hz -44 @1kHZ -68 @1MHz	-63 @10Hz -53 @1kHZ -81 @1MHz	-45 @100Hz	-93.3 @10Hz -70 @1kHZ -57 @1MHz	-83 @DC	N/A	-80 @1kHZ
Line Regulation (%/V)	0.37	0.4	0.002	0.003	0.0041	N/A	0.001
Area (mm^2)	0.079	0.038	0.055	0.015	0.0616	0.145	N/A

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